A Survey on Heuristic Algorithms on Detailed Routing in Physical Design Automation

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Abstract— Routing is one of the most complex stage in physical design. Detailed routing determines the exact place of tracks and via. The main objective ofdetailed routing is to reduce the area of an integrated chip . Minimization of wire length,number of tracks, channel length, congestion factor is the key problem in physical design. Routing is a process to interconnect all the nets within the channel considering all constraints(horizontal and vertical constraints) of that channel. Unlike traditional routing schemes ,all the traffic is along a single path, multipath routing scheme splitthe traffic among several paths in order to reduce the congestion. In this paper, we analyze different single-layer algorithms, two-layer algorithms and three layer algorithms and conclude that the objective of the routing problems like crosstalk, wire length, channel length, no of tracks and vias.

Index Terms— Algorithm, Detailed routing, Physical design, VLSI CAD

I. Introduction

The most important step in the physical design of VLSI circuits is detailed routing. Detailed routing determines the exact tracks and via for nets. The two most popular types of detailed routing: channel routing and full-chip routing. In earlier process technologies when the maximum number of available metal layers was only two or three, channel routing was pervasively used, because most wires were routed in the free space(i.e. routing channel) between a pair of logic blocks. In modern technologies, a chip typically contains six to ten metal layers, and the number of available metal layers is expected to increase steadily in the near future. With more metal layers, routing over the logic block is common. As a result, routing regions become more like channel-less regions. This trend drives the need of a full-chip routing.

Channel routing plays a important role in a physical design of VLSI chips. Many algorithms have been proposedin the past few years, for single-layer routing [15] and two-layer routing and three-layer routing. Recent studies shows that the network would be more efficient and robust if routers could flexibly divide traffic over multiple paths. Distributed multipath routing algorithm solve the question of path selection and minimize congestion[20]. Crosstalk minimization is done by bubble sorting based manhatten channel router and rerouting algorithm in four-layer non-manhattan channel routing[28].

The remainder of the paper is organized as follow: section II describes the evolution tree of detailed routing and algorithms in detailed routing. In Section III, we present our survey work.Finally , we conclude our work in section IV.

II. Detailed Routing - The Evolution Tree

Detailed routing problem is solved by solving one routing region at a time. The routing area is first partitioned into smaller regions. Since, the global router only assign wires to different regions, the detailed routing problem is to find the actual geometric path for each wire in a region. Shape of the region is the most important factor.

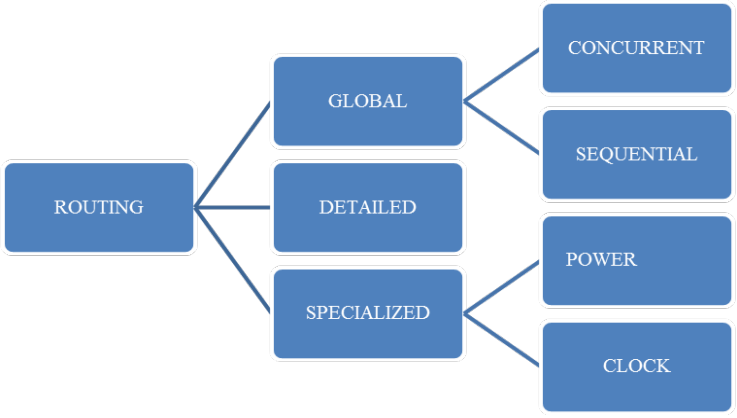

Fig. 1. Routing Flow

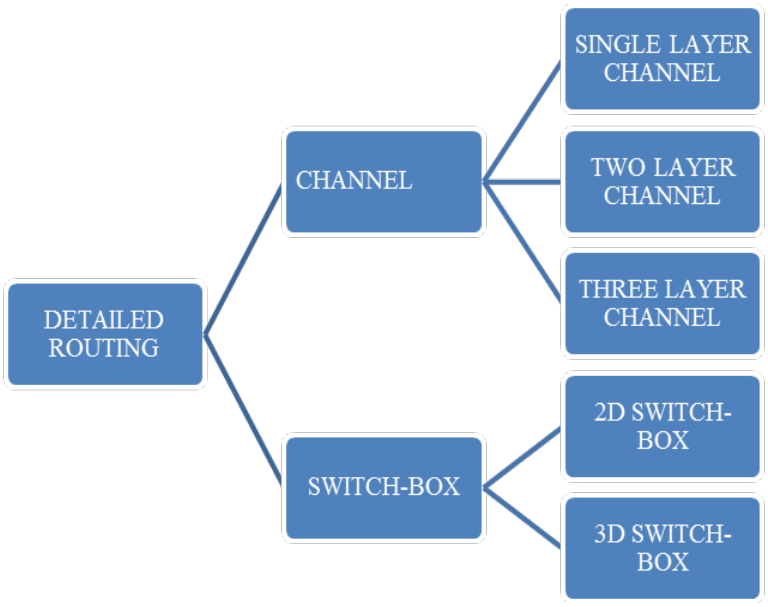

Fig. 1a. Detailed Routing

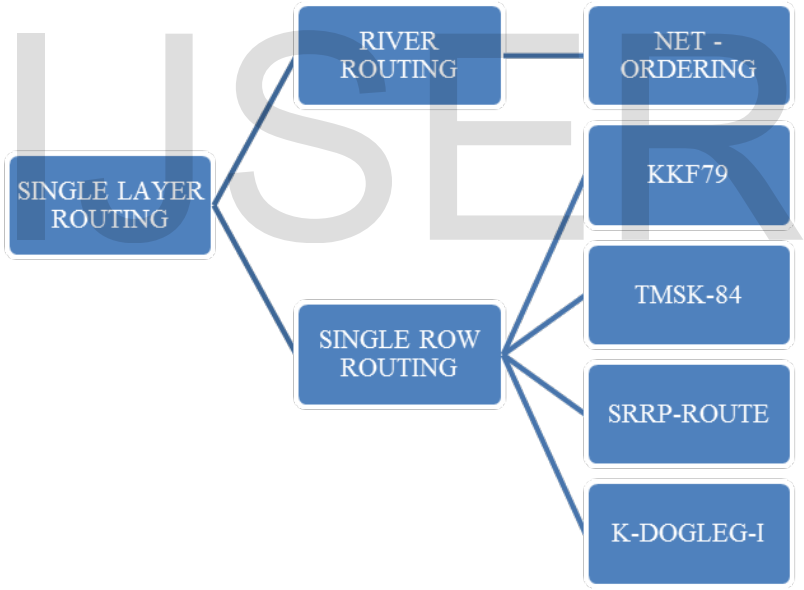

Fig. 1b. Single Layer Routing

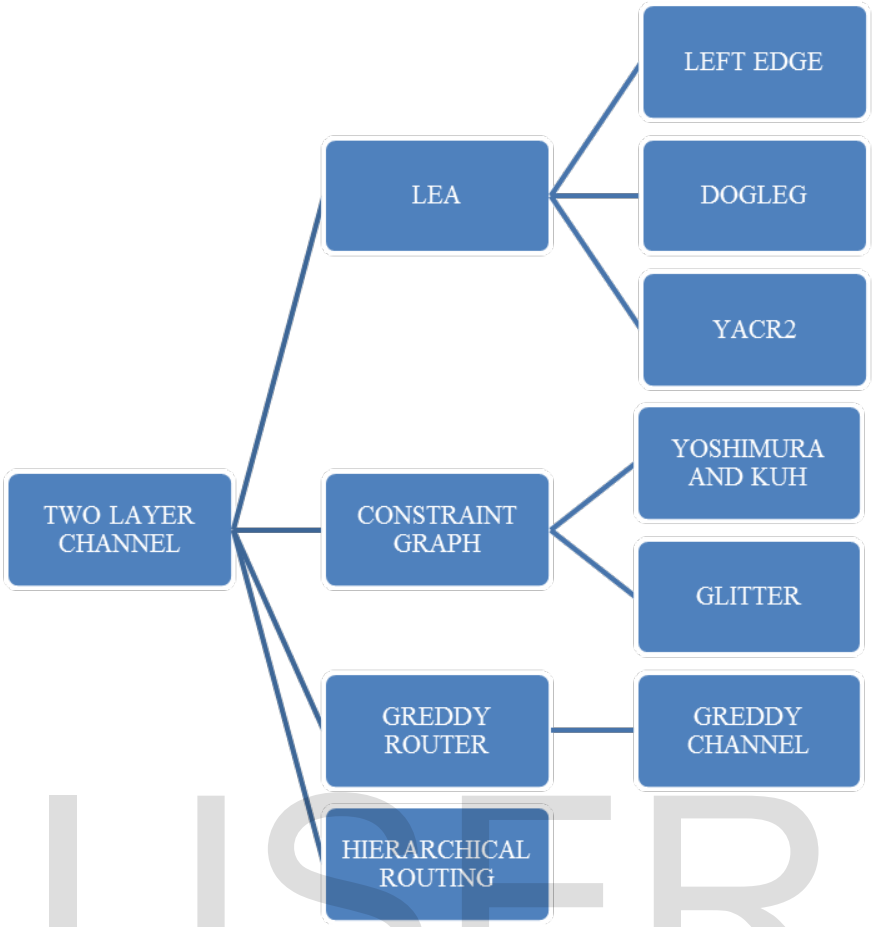

Fig. 1c. Two Layer Routing

Detailed Routing Algorithms

.LEA The algorithm was designed to route array-based two layer PCBs. It uses a reserved layer modelit doesnot allow doglegs and any vertical constraints.

ii.DOGLEG Drawback of LEA is overcome by this algorithm. The dogleg router isthatit allows multiterminal netsand vertical constraints.

iii.YACR2 This algorithm explain how vertical constraints violation are handled and define the concept of verticaloverlap fac tor, which indicate the total number of tracks that a vertical constraint violation spans.

iv. Y-K It is based on net merging. It include both horizontal and vertical constraints graphs and assign tasks to nets so as to minimize the effect of vertical constraint chain in the vertical constraint

v. GLITTER A grid-less variable-width channel router called glitter. Glitter can utilize multiple layer technology.

vi. GREEDY The algorithm start from the left most column and place all the nets and segments of a column beforeproceedings to the next right column. In each column, the router assigns net segments to tracks in a greedy manner.

III. Literature Survey

PAPER TITLE AND AUTHOR	YEAR JOURNALS CONFERENCE	LANGUAGE, TECHNOLOGY AND EDA	METHODOLOGY	PARAMETERS - WIRE LENGTH -NO OF TRACKS CHANNEL LENGTH	ACHIEVEMENTS	LIMITATIONS/ TRADEOFF	FUTURE SCOPE	REMARKS
"A New algorithms with Minimum Tracks for Four Layer Channel Routing in VLSI Design"Ajoy Kumar Khan , Bhaskar Das [1]	2013 IEEE ICCCI	C Programming language	Vertical Constraint Graph(VCG), Horizontal Constraint Graph(HCG) Horizontal non Constraint Graph(HNCG)	50% of reduction in number of tracks	Reduced the no. of tracks needed for channel routing problem then automatically the area of an IC chip is also reduced	There is no close loop in the VCG of that channel that means the VCG must be tree	If there is a cycle in VCG. a) Add a vertical layer. Then it becomes a five layer channel problem. So we draw some algorithms for this purpose.	a) Know about transitively oriented graph. b) reduction the no of tracks gives good result
"Yet an Efficient Algorithm for Computing Reduced Area VLSI Channel Routing Solution With Floating Terminals "Achire Pal, SwagataSahaSau, TarakN.Mandal et-al.[2]	2011 IEEE Proceedings of 14th IC-CIT	C programming language	Vertical constraint graph(VCG), Horizontal non constraint graph(HNCG)	Density of the channel = no. of tracks required	Reduction of area or the channel width	--	The algorithms for completing routing solutions with reduced wire length and doglegging	a) NP problem is solved by proposed algorithm. b)reduction channel area under the reserved two-layer Manhattan no-dogleg channel.

"A Graph Theoretic Approach to Minimize Total Wire Length in Channel Routing"Pralay Mitra et. al [3]	2003 IEEE	--	Using TAH framework, reduction the total wire length.	--	Minimization of total wire length for two layer channel routing.	Does not use back-tracking	a) extension to computer reduced wirelength routing solution in the reserved three-layer HVH and VHV routing models.	This algorithm does notuse much area in computing such solution.
"An Efficient High Performance Parallel Algorithm to Yield Reduced Wire Length VLSI Circuits". SwagataSahaSau, Rajat Kumar Pal [4]	2012 IEEE 5th CODEC	C++	High performance parallel algorithm MTAH is computation by small small modules.	For r2: 21.03% Ex5: 27.97% Reduction in total wire length in a solution computed using our algorithm MTAH	Different modules of MTAH run in parallel so it requires less execution time and reduces the total wire length.	Algorithm require constant number of processor (or a single processor)	Computing reduced wire length routing solution in the reserved three and multi-layer no-dogleg as well as and dogleg routing modules.	a) In which computation time is negligibly small b) MTAH requires one ,two or three tracks.
"A Firefly Algorithm Approach for Routing in VLSI" M.NasirAyob, Fariz Hassan,et-al. [5]	2012 IEEE ISCAIE	Visual basic 6, Use size of 22* 17 grids.	Delay model Elmore delay Calculation and grid-graph model	The optimal solution of the case study which is 571.73ps	Find minimum time delay by choosing the path and placing the buffer intelligently	--	Using other optimization techniques such as magnetic optimization algorithm and paddy field algorithm.	Examine the fitness of new firefly and updating the light intensity.

"A Routing Framework for Delay Tolerant Networks Based on Encounter Angle "Yue Cao, Haitham Cruick-shank, Zhili Sun. [6]	2011 IEEE	C++ lan-guage	a) Calculation of the encoun-ter angle. b) Probabilistic replication c) Routing framework	--	Reduces the num-ber of aborted messages due to mobility factor and achieves the signif-icant per-formance	--	a) More intelligent mechanism for the routing framework - b) optimize the estima-tion of po-tential en-counter duration with low complexity.	a) battery con-sumption function is also integrated into algorithms b) reduce the no. of transmissions for efficient bandwidth usages.
"Encounter-Based Routing in Delay Tol-erant Net-works" Jun-baozhang,G uangchun-lua, Ke Qin Haifeng Sun. [7]	2011 IEEE	Oppor-tunistic network envi-ronment (ONE) simula-tor ver-sion 1.4.0	Simulation set-up Effect of trans-mission range Effect of stor-age capacity	--	EBR has good per-formance and low overhead in sparse network.	--	Analysis to real mobili-ty traces and hetero-geneous networks.	EBR exploits inter-contact time to predict the no of contacts from now to the expected delay.
"GDRouter: Interleaved Global Routing and De-tailed Rout-ing for Ul-timate Routabil-ity"Yanhen g Zhang Chris Chu. [8]	2012 DAC	C lan-guage	GDRouter a)Fast route(global) b)Regular route(detailed)	Reduce number of unassigned global segment by : a) 90%for ISPD98 b) 60%for ISPD05/06	Enhanced routability	GDRout-er quits the loop if de-tailed routing routabil-ity stops improv-ing or reaches max. iteration.	The solu-tion quality of the inter-leaved global rout-ing and detailed routing algorithms.	a) spine routing and virtual routing are applied to gen-erate initial global capacity. b) GDRouter: an interleaved global and detailed rout-ing algorithm for the ultimate routa-bility.
"A Novel Detailed Routing Algorithm with Exact Matching Constraint for Analog	2011 IEEE 12th Int'l Symposi-um on Quality Electronic	C++ lan-guage run on Linux server with Intel(R)	Detailed rout-ing: a) Grid algo-rithm b) Gridless algorithm	10X speedup	Size of the routing area with the exact matching con-straints is often	--	Algorithm to consider shielding and other geometric constraints.	Investigation of bounded-error matching routing beyond the exact matching routing.

and Mixed Signal Circuits"Qiang Gao,Hailong Yao Qiang-Zhou,YciCai. [9]	Design	Xeon(TM)300 GHZ CPU			small enough to directly apply detailed routing			
"Dangling-wire Avoidance Routing for Crossbar Switch Structured ASIC Design Style"Yi-Huang Hung Hung-Yi Li , Po- Yang Hsu ,Yi-Yu-Liu. [10]	2010 IEEE Work is supported in National Science Council of Taiwan	--	Steiner three construction: a)Pin assignment b) Dangling wire aware c) Anchor pair insertion for congestion removal	21% dangling wire 34%channel width 13%total wire length	Crossbar switch routing framework reduces: a) dangling-wire b) total wire length c) routing congestion.	--	--	Proposed a) a high speed crossbar switch routing framework b) graph model for crossbar switch routing.
"Graph Colouring Based Multi Pin Net Detailed Routing for FPGA using SAT" Shyamapada Mukherjee, Suchismita Roy [11]	2013 IEEE 3rd IACC	C programming language	Modeled the FPGA as a colourablegraph . Demonstrated SAT-based FPGA detailed routing	Minimization of channel width	--	Consider all multi-pin nets simultaneously	--	Net ordering is a big issue in the net at a time approach because invalid sequence of net-selection may cause the algorithm to fail.
"The Automation design Based on Graphs for the Symmetrical Routing in Integrated Circuit" Xu-	2011 IEEE 2011 International Conference on System Science, Engineering De-	C programming language	a) Theorems b) Algorithms c) Corollary d) Conjecture	--	A new heuristic algorithm based on the conclusion to solve the problem of 2-layer manhattan	a) Vertical constraints are noncyclic b) extra empty columns and dog-	--	The minimum parallel clique cover of CCG is equal to the optimal solution of 2-layer manhattan channel routing.

Zhenghua. [12]	sign and Manufac-turing Informati-zation				channel routing	legs are not al-lowed		
"Crossing-Aware Channel Routing For Photon-ic Wave-guides" Christopher Condrat, Priyank-Kalla, Ste-ve Blair. [13]	2013 IEEE	--	--	a) CA(crossing-aware)reduces the no of cross-ing to 0.607 × produce by YK(Yoshimura-Kuh)router b) cost of rough-ly 1.25×no of tracks.	--	Cross-ing-minimi-zation-comes at the cost of addi-tional tracks.	--	a) It uses left edge-style channel rout-ers. b) signal losses is reduced by channel router.
"Analytical Placement of Mixed-size Cir-cuits for Better De-tailed-Routabil-ity" Shuai-Li ,Cheng-KokKoh. [14]	2014 IEEE	--	Main two Con-tribution are: a) A new ana-lytical place-ment formula-tion with pin density con-straints b)scaled smoothing method to cope with fixed mac-ro blocks.	a) avgwire-length& via count are 4% smaller than rip-ple &simPLR b) compared with NTUplace4 : - avg wire length:1.9% larger - avg via count 1.0%smaller	Technique are effec-tive in improving the routa-bility of placement results.	Target density t_{den} is set to be 0.80	--	Detailed routing solutions with few-er violations can be generated in a shorter time for the proposed place-ment

"Short - Term Hydrothermal Dispatch With River-Level and Routing Constraints."Andre LuizDiniz, Thiago Moto Souza. [15]	2014 IEEE Transactions on Power Systems	--	a) Short -Term Hydrothermal Dispatch problem. b) River Level Constraints. c) River Routing Constraints.	--	High accuracy of proposed approach to represent maximum hourly and daily river-level variations without increase in CPU time	--	This approach to be used as a guideline for actual system operation.	Requirement: a) hydro plants b)thermal plants c) high accuracy
"Efficient Routing in heterogeneous SoC Designs with Small Implementation overhead"Jose Cano, JaseFlich et al. [16]	2014 IEEE Transactions on Computers	--	a)LBDRx is a series of routing mechanisms b) A mapping tool	Minimize the overall cost	Reduce the size of routing tables either at end nodes or at routers.	Reduce logic cost, regardless of system size	Further explore the mapping tool focusing on performance issues and to optimize the tool to provide the best mapping for the target app.	Routing tables were replaced by the LBDRx mechanism.
"A Boolean Rule-Based Approach for Manufacturability-Aware Cell Routing"Jordi Cortadella, Jordi Petit. et al. [17]	2014 IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems	--	IPL(integer linear programming) and LNS(large neighborhood search) algorithm for routing optimization	Wire length reduction = 1.6%	Reduced logic cost regardless of system size.	Performance, power, area	This EDA tool will enable the exploration and characterization of wide range of layout templates for cell libraries.	The main reduction was in horizontal and vertical, but this reduction was compensated by an increase of vertical and increase of vias.
"An Efficient intersection Avoiding Rectilinear Routing Technique in VLSI" Pratha-	2013	C language	Two approaches: a)Sequential b)Concurrent	a)15% reduction in wirelength b) reduces CPU execution time.	a)Improved intersection between nets and congestion b)Minimized block-	--	Delay and Crosstalk can be reduced and pin multi net routing using non manhattan	To avoid blockage during routing Weight-based steiner edge technique used.

pratimsaha, suman-tasaha,andt uhinasa-manta[18]					age in routing		routing	
"Regular Route : An Efficient Detailed Router Applying Regular Routing Patterns"Yanheng Zhang Chris Chu. [19]	2013 IEEE Transactions On Very Large Scale Integration (Vlsi) Systems	--	a)Algorithm proceeds in a bottom-up layer -by- layer manner : a) Local net routing b) Global segment assignment c) Optimization	20%-30% less metal 2 usage	a)Effectiveness and Efficiency of Regular Route. b)Minor impact for density control	4 * 4 G-cell to form one region.	a) Improve the performance of Regular Route b) A parallel version of tool for further runtime reduction.	
"A Distributed Multipath Routing Algorithm To Minimize Congestion" GuoXin, Zhang Jun, Zhang Tao. [20]	2009 IEEE 28th Digital Avionics Systems Conference	--	Distributed Congestion-Minimized Multipath (D-CMM):- a)Congestion facto b)Network throughput c)Delay	Congestion factor < 1.0	a)Increase network throughput b) Decrease congestion factor c)Increase of shortest path delay	Transfer delay	--	Proposed algorithm is more suitable in long distance transmission and dense network topology.
"A Fast Placement and Global Routing Integrated Algorithm for Hierarchical FPGAs" Limin Zhu, Jinan Bian,Qiang Zhou ,YieiCai. [21]	2011 International Conference on Information Science and Technology	C++ programs including netlist file	For reduction of mismatch in HFPGA : a) New Placement b) New Global Routing c) Detailed Routing	Alu4 : 3.98(CPU/s) Seq : 3.96(CPU/s) Frg1 : .011(CPU/s)	CPU time get larger very slowly as the circuit become larger.	--	--	A placement and global routing algorithm is presented to solve the mismatch problems between the two FPGA.

"A Fast Recursive Detailed Routing Algorithm for Hierarchical FPGAs" Limin Zhu, Jinan Bian,Qiang Zhou ,YieiCai. [22]	2011 15th International Conference on Computer supported Cooperative Work in Design	C++ programs including netlist file	Algorithm for hierarchical FPGAs (HFPGAs): a)Architecture b)Switchbox Connection Patterns c)Validity of Recursive Routing	Alu4 : 1 Rep Seq : 2 Rep Frg1 : 0 Rep * Rep: count of repetitions	CPU time get larger very slowly due to its recursive nature	--	--	A recursive detailed routing is presented to specifically solve the routing problems for hierarchical FPGA
"A Two-Step Heuristic Algorithm for Minimum-Crosstalk Routing Resource Assignment" Yicicai,Bin Liu,Qiang Zhou, Xianlong Hong. [23]	2006 IEEE Transactions on Circuits and Systems—II	C++	Two stage algorithm for crosstalk minimization in an integrated routing resource assignment stage between global & detailed routing.	--	Reduce the crosstalk.	Reduce crosstalk as well as increase the completing rate.	Wire sizing/spacing introduce into our framework.	Two criteria are used to measure the crosstalk across the chip : a) no of segments that are sensitive to each other and placed adjacently b) no. of failed segments
"Double Patterning-Aware Detailed routing with Mask Usage Balancing" Seong-I Lei,Chris Chu, Wai-Kei Mak. [24]	2014 IEEE	C++ Programming Language 32nm and 22nm technology	-Double patterning lithography(DPL) -Maze Routing with Stitch Minimization -Negotiated Congestion based rip-up and reroute	For non- preferred routing: ->1.9% : shorter wirelength ->85.2% less stitches -> 18.8% more vias ->98.2% less coloring conflicts For preferred routing:	a)Faster b)Improvement on the number of stitches	Stitch_cost =30 Via_cost =10 $\alpha = 0.49$ Targeted range 0.49-0.51	TPL or multiple patterning lithography in detailed routing algorithm.	First fix the color of each track in the routing grid and perform detailed routing using these pre-colored tracks.

				->0.2% : shorter wirelength ->9% less vias				
"DFM Based Detailed Routing Algorithm for ECP and CMP" Yin Shen, YiciCai, Qiang Zhou, Xianlong-Hong . [25]	2008 IEEE 9th International Symposium on Quality Electronics Design	--	CMR algorithm has main two steps: a) maze searching step b) maze backtracking step.	CMR vs MR 14.6% metal density 0.96% avg amount of dummy fill CMR vs DMR 6.99% metal density 0.72% avg amount of dummy fill	a) increase total wirelength b) total number of vias	Minimizing the metal density and the amount of dummy fill metal while the wire length and vias are not increased	More accurate ECP and CMP model into the routing algorithm.	a) Consider metal density . b) flatness of chips and improve the yield of semiconductor.
"Detailed-Routing Algorithms for Dense Pin Clusters in Integrated Circuits" Muhammet Mustafa Ozdal. [26]	2009 IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems	C++ GNU Linear Programming Kit	a) A polynomial-time optimal algorithm b) An MCF-based model c) An LR-based algorithm	78% reduces the number of final opens Avg via counts per net by 4% 34% decrease the total execution times	a) reduce the number of nets b) CPU-time requirements increase with increasing cluster size	--	--	

"An Integer-Linear-Programming-Based Routing Algorithm for Flip-Chip Designs" Jia-Wei Fang, Chin-Hsiung Hsu, Yao-Wen Chang. [27]	2009 IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems	C++ program gramming language	Three reduction technique on the problem size: a) Constraint-graph-based pruning b) ILP node merging c) ILP edge bounding	ILP node merging: Reduce the variables (constraints) by avg 84.0%(97.9%) ILP edge bounding: Reduce the variables (constraints) by avg7.0%(9.5%)	RDL router for the flip-chip(FC) package minimization are: a) signal skews b) wire widths c) total wirelength	--	--	
"Crosstalk Minimization in Four-Layer Non-Manhattan Channel Routing" Yongbin Yu, Bo Yang, Xuliang-Zhang,Jueb ang Yu. [28]	2004 IEEE	C++	Two algorithms are followed : a) An improved bubble sorting based non-manhattan channel router b) A rerouting algorithms	reduce the crosstalk by an average of 27.9%	Minimization of crosstalk	--	--	Solve the gridded non-Manhattan channel routing problem with the consideration of crosstalk by modifying the existing bubble-sorting algorithm
"Algorithms for High performance Two-Layer Channel Routing" Achira Pal,Debojit Kundu, et al. [29]	2007 IEEE	--	Algorithms for crosstalk minimization: a) Track-interchange(for simple channel instances) b) Track interchange(for simple channel instances)	30.77% reduced crosstalk	Reduction of crosstalk	--	Algorithm for reducing crosstalk for three-layer HVH routing model could be devised	Firstly Algorithm Net- Change after that Track - Interchange is consider, so dependence of algorithm is there.

"Channel Based Routing in Channel-less Circuits" Glau-GlaucoBor-coBor-gesValim dos Santos, et al. [30]	2006 IEEE	JAVA 0.35µ tech-nology	ChAOS ("chan-nel assignment toward full-OTS synthesis") router	0.6% increase in wirelength 7.2% increase in area	Concen-trate in develop-ing tools that run very fast and can be used in a straight forward conver-gent methodol-ogy for layout generation	No two pins in same row can have the same x coordi-nate	a) three or more layer together with some optimiza-tion in data structures b) fast stei-ner tree heuristics be consid-ered at global planning for wire length re-duction	Aligned Terminals RoutingModel (ATRM) in which channel routing algorithms can be used to make con-nections.
"Via Mini-mization For Multi-layer Chan-nel Routing in VLSI Design" Bhaskar Das, Ashim Kumar and Ajoy Ku-mar Khan[31]	2014 IEEE Fourth Interna-tional Confer-ence on Commu-nication Systems and Net-work Technolo-gies.	--	a) Two layer channel: - genetic algo-rithm - with layout modification b)Three layer channel: - with layout modification -with three lay-er channel rout-ing -using BFS	Reduction of vias Layout modifica-tion : 34% Using BFS :more than 12% nd less than 55%	Reduce the num-ber of vias without increasing the rout-ing area.	--	Develop an algorithm for via minimiza-tion prob-lem.	a) Based on breadth first search b) no specific rule for layering.
"Digital Implemen-tation of 16-bit Syn-chronous Counter with SoC Encounter for Place-ment and Routing" Pillem Ramesh and Venka-	2012 Interna-tional Journal of Engineer-ing Re-search and Applica-tion (IJE-RA)	SoC Encoun-ter 130 tech-nology	a) floor plan-ning b) power stripes c) placement d) generation of clock tree. e) detailed rout-ing.	Setup slack: 0.034ns Hold slack : 0.016ns Density : 90.079%	No DRC violations.	--	--	Helps physical designer to assess partition the logical hierarchy and ana-lyzing the optimal pin assignments time budgeting, power grids

taAravindBezawada[32]								
"Restorable Routing Algorithm in optical Networks by Reducing Blocking Probability"Raman Kumar and Navneet-Kaur[33]	2014 IEEE Proceedings RAECS UIET Punjab University Chandigarh	--	Routing algorithms: a) WLCR-FF(weighted Least Congested Routing - First fit) b)shortest path routing algorithm c)genetic algorithm d) Minimum marginal cost routing algorithm.	Blocking probability : -proposed algorithm 8.6431×10^{-9}% Conventional algorithm 4×10^{-2}%	Blocking probability of the network for proposed algorithm increased with the increase in the offered load per unit link.	--	--	Number of light paths is becoming the main factor in determining the cost of WDM network.
"A Hierarchical Genetic Algorithm for Multi-Layer Channel Routing" Mark P.Cloyed and Hesham H. Ali[34]	2004 IEEE	--	Hierarchical Genetic Algorithm.	Parameter was incremented from initial value of 2 to a final value 11.	Algorithm utilized the multiple layers to remove vertical constraints and overcome the vertical constrained cycles.	--	--	This is the algorithm which is applicable for multi-layers. (2Lyr, HVH, VHV)
"Channel/Switchbox Definition for VLSI Building-Block Layout" Yang Cai and D.F.Wong	1991 IEEE Transactions on computer-aided design.	Pascal language.	Comparison of : Greedy algorithm and Minimum feedback vertex set algorithm.	No of Switch-boxes is at most 2 more than the optimal value	No of switch-boxes generated by our algorithm is only about half as greedy algorithm	--	Better algorithms can be developed to minimize the number of L-shaped channels used	Computation time for large examples are only a few seconds.

[35]								
"High Performance Multi-Layer Routing for VLSI Circuit Synthesis" Sangram-jitBhowal , rajat K. Pal [36]	2004 IEEE	--	MCCI Routing solutions: a) two layer VH b)three-layer VHV and HVH c) four layer VHVH	Crosstalk is reduced from 9 unit to 7 unit .	Minimize routing area and reduce total crosstalk in computing a routing solution.	--	Reduce total wire length required in a routing solution that may optimize signal delays.	Amount of crosstalk between wire segments is proportional to the coupling capacitance.

IV. CONCLUSION

In this paper a comparison on routing problems likeNP-hard andNP-complete based on different algorithms is done. We conclude that if the layers are increased than the number of tracks are reduced so that the NP-complete problem is solved and crosstalk is reduced. 50% ,reduction in number of tracks, 30.77% reduced crosstalk[29]Gridless routing algorithm is much faster than grid routing algorithm(i.e around 10× speedup)[9]. These are the categories of manhattan channel routing. In channel-less circuits, channel based routing increase in wirelength and area.

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